A Broadband Upconverter Unit for a Cable-Modem Double-Conversion Receiver

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Abstract — **A broadband upconverter unit for double-conversion receivers used in cable modems is presented in this paper. The unit includes a variable-gain low-noise amplifier, a double-balanced mixer, a three-stage VCO bank for LO generation and a divide-by-two circuit for driving an external PLL. The unit upconverts a 6- or 8-MHz channel from 47-862 MHz input band to around 1575 MHz intermediate frequency. In experimental testing the unit measures over 20 dB gain with 8-dB noise figure and 15-dB gain tuning. The unit is implemented in a 0.9-μm SiGe bipolar process.**

I. Introduction

In broadband communications systems, for instance in HDTV, DVB or cable-modem applications in hybrid fiber-coax (HFC) networks, a double-conversion receiver architecture is often employed [1]. In such a receiver a channel from a broad input band is first upconverted to a constant first IF, where filtering takes place, and then the signal is downconverted to a second IF. In the DOCSIS (Data-Over-Cable Service Interface Specification [2]) system, the input band is 47-862 MHz, and the second IF lies at 36 MHz (European standard) or at 44 MHz (US). An arbitrary first intermediate frequency can be selected as long as it is above the specified frequency band. The higher the first IF is, the smaller relative tuning range is required from the LO1 source. Double-conversion receiver architecture, depicted in Fig. 1, offers potential for higher integration and thus lower component count compared to the alternative approach, a receiver based on tracking filters [3]. The advantages of double-conversion receiver are flat IF response, better selectivity, good broadband impedance matching and high image rejection [4]. Furthermore, oscillators operate above the input band. Thus, contamination of the cable network is avoided with a good input match over the entire band to avoid

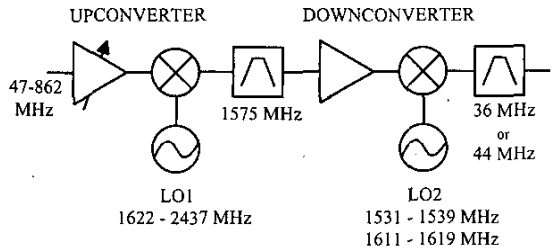

Fig. 1. Double-conversion RF tuner.

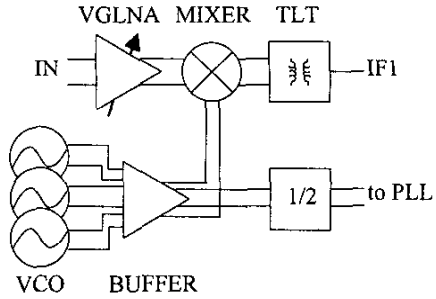

Fig. 2. Block diagram of the implemented upconverter unit.

reflections and low in-band leakage. In our system plan the first IF is 1575 MHz allowing us to use readily available low-cost SAW filter meant for GPS applications. The first local oscillator signal (LO1) ranges then from 1622 to 2437 MHz. As the complete input band, for instance consisting of as many as 130 6-MHz channels, is entering the upconverter without any pre-filtering, high linearity is required. The provided signal levels are from –15 to +15 dBmV and in our approach the gain is reduced on dB-to-dB basis from 0 dBmV input level. Thus, a demand for continuous gain tuning is 15 dB. Finally, for maintaining adequate signal-to-noise ratio, a 9-dB noise figure in the high-gain mode is required.

In this paper we are describing a prototype design for a DOCSIS compatible cable modem RF tuner upconverter

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unit. The downconverter unit is described in ref. [5]. The circuits are designed for and fabricated in a 0.9-μm SiGe bipolar process. The circuit design aspects are discussed in the next section. Then, experimental results are given, and finally some conclusions are drawn.

II. Circuit Design

The upconverter unit, shown in Fig. 2, consists of a variable-gain low-noise amplifier, a double-balanced mixer with open-collector output, a three-unit on-chip voltage-controlled oscillator bank with a buffer, and a divide-by-two circuit for feeding an external dual-PLL. At the output, differential-to-single-ended conversion is done with an external transformer (TLT). At the input, single-to-differential conversion is also done on board.

A. Variable-Gain Low-Noise Amplifier

Variable-gain low-noise amplifier (VGLNA) is a resistively matched balanced single-stage amplifier. It is depicted at left in Fig. 3. By using resistive matching we are able to meet the required gain and noise figure while maintaining a good impedance matching to 75 Ω over the entire input band. Linearity is improved with small emitter degeneration resistors, unfortunately with slight penalty on noise figure. Gain tuning is achieved by using a current-steering approach. Part of the signal is fed to the supply rail instead of the load resistors by altering the biasing of the current-steering transistors. The current-steering scheme does not alter the operation of the actual amplifying transistors. Thus, impedance matching and input-referred linearity remain constant. The weakness of the current steering approach is that output-referred linearity (OIP3) does not remain constant. Since the OIP3 requirement has to be met in the low-gain mode as well, linearity is unnecessarily good in the high-gain mode and current consumption is high. Second-order nonlinearity (OIP2) is handled by drawing the layout as symmetric as possible. The main source of OIP2 degradation is resistor mismatch in this circuit.

B. Upconversion Mixer

Mixer is a traditional double-balanced Gilbert-cell mixer with a resistive emitter degeneration for improving the linearity. However, gain is reduced and noise increased with increased degeneration resistance. The output of the VGLNA is DC-coupled to the mixer input, so the transconductance stage is biased with the common-mode voltage of the VGLNA output. Special care was taken that correct biasing remains regardless of gain tuning or process spread. The mixer has an open-collector output, so there is no need for output buffers. The benefit of the open-collector output compared to the output buffers is lower power consumption and improved linearity, since the buffers limit the linearity of the system. The circuit schematic is depicted at right in Fig. 3.

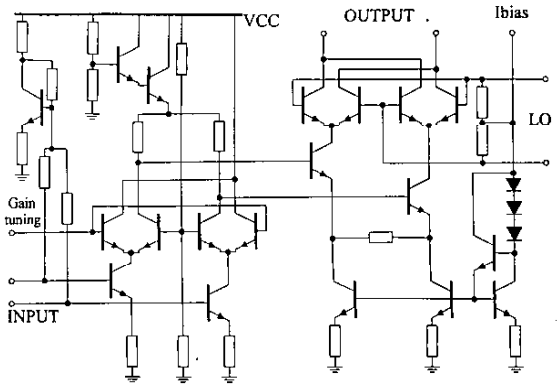

Fig. 3. VGLNA at left and mixer at right.

C. Transmission Line Transformer

As the mixer has an open-collector structure, the transformer is an essential part of the circuit designing. The output impedance matching of the upconverter is done with a transformer, parallel inductors and series capacitors. The transformer is also needed to make the differential-to-single-ended conversion required by the first IF filter. The transformer is a transmission line step-up transformer (TLT) with 1:4 impedance ratio. We have developed an RLCM-type equivalent circuit for the transformer, as depicted in Fig. 4, for achieving high performance and reliable design. A lumped element model is applicable also in time-domain simulators.

D. Triple-VCO

Design strategies for a wide-tuning-range LC-VCO with the process applied here was thoroughly described by us in the previous RF IC symp. [6]. We found out that with this technology the layout parasitics have a severe impact on the VCO characteristics. Therefore, instead of a dual-VCO, a three-unit VCO bank is required to cover the required band with a sufficient margin for process spread etc. Briefly: a single LC-VCO is depicted in Fig. 5, and in it, the required negative conductance is created with a cross-coupled pair. The three oscillators in Triple-VCO differ only by the inductance value, which is used for tailoring the oscillators to the correct frequency band. An external bias current is used for selecting the active oscillator.

E. Buffer

Buffer is used for isolating the mixer, Triple-VCO and frequency divider. One branch of the buffer is biased from the active oscillator and the other two branches are inactive. This way we are combining the outputs of the three VCOs. Divide-by-two circuit is driven directly from the load resistor node, while emitter followers provide low-impedance source to the mixer LO port. Simulations show that it is a critical arrangement for mixer linearity. The schematic of the buffer is shown in Fig. 6.

F. Divide-by-Two Circuit

Divide-by-two circuit includes two common-mode logic (CML) latches in an astabile loop as depicted at left in Fig. 7. A CML latch is shown in Fig. 7 right. The divide-by-two circuit is followed by a buffer stage used for driving an external PLL in a 50-Ω environment. According to the simulations, the input-referred speed of the divider exceeds 3.3 GHz with worst process-spread corner parameters.

III. Experimental Results

Circuits were fabricated in a 0.9-μm SiGe HBT process and the test dies were encapsulated in SSO36 package. The microphotograph of 2.4-mm^2 die is shown in Fig. 8. Major measurement results are collected into Table 1, and are given in the high-gain mode and in the 15-dB reduced low-gain mode. Characteristics decline monotonically with the gain tuning, and hence, here two modes are sufficient. Also, characteristics are given in the beginning (47 MHz), in the middle (450 MHz) and at the end (862 MHz) of the band. Fig. 9 depicts gain and noise in the high-gain mode over the DOCSIS band. Linearity was measured with a traditional two-tone test with 6 MHz spacing for test tones. Results in the high-gain mode are depicted in Fig. 10. Here second-order intermodulation product at the output is for tone $f_{LO}-(f_1-f_2)$. If the selected tone is $f_{LO}-(f_1+f_2)$, the OIP2 result is about 10 dB better. Main concern is that the linearity in the low-gain mode is not good enough. This is caused by the fact that part of the signal is fed to the supply rail and there is not sufficient amount of de-coupling capacitor, ie. the impedance of the supply rail is too high. The test circuit includes an additional output for measuring Triple-VCO characteristics and Fig. 11 shows Triple-VCO frequency tuning characteristics. The proper operation of the divider was checked by measuring Triple-VCO characteristics from the PLL output as well: divide-by-two function worked over the complete Triple-VCO frequency range with a sufficient output power for driving the PLL, and phase noise was improved by 6 dB as it should.

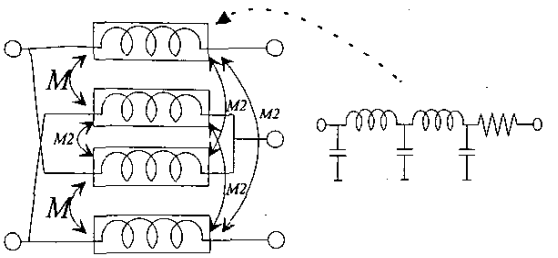

Fig. 4. Model for the transformer. Each winding is represented with a distributed LC-line. Primary mutual coupling is denoted with "M" and weaker parasitic coupling with "M2".

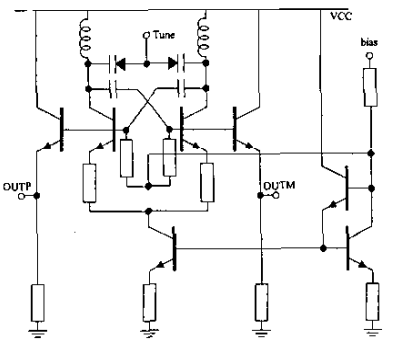

Fig. 5. Voltage-controlled oscillator.

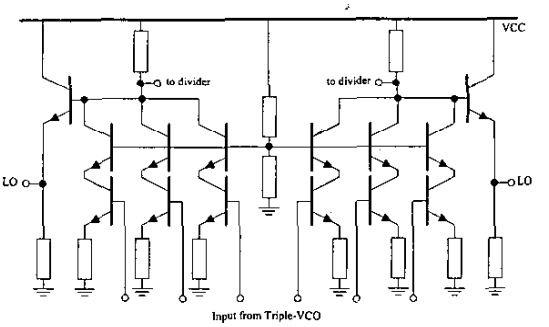

Fig. 6. Buffer for combining the VCO outputs.

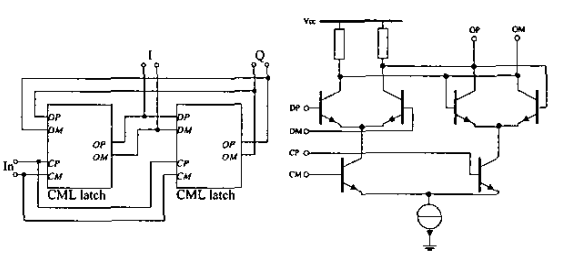

Fig. 7. Divide-by-two D-flipflop and CML latch.

IV. CONCLUSIONS

In this paper design strategies for an upconverter unit for a double-conversion cable-modem RF tuner are discussed, and a design of a prototype circuit is described. The main challenges lies in broadband issues: high linearity as well as good matching and noise figure are required in the entire band of 47-862 MHz. Furthermore, large tuning range in conjunction with low phase noise sets challenges for the VCO designing. The present prototype has sufficient gain and noise figure as well as properly operating gain tuning.

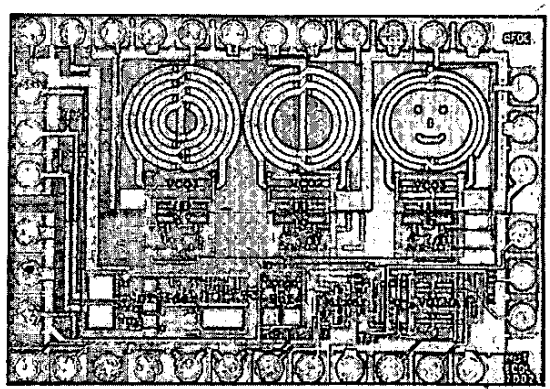

Fig. 8. Die microphotograph: die size is 2.4 mm^2.

TABLE I.
Measurement results from a typical sample.

Input band	47 – 862 MHz		
Output frequency	1575 MHz		
Supply voltage	5 V		
Current cons.	49 mA		
High-gain mode	47 MHz	450 MHz	862 MHz
Gain [dB]	24.1	23.5	22.5
Noise figure [dB]	6.7	7.1	7.7
Input matching [dB]	-23	-18	-14
Linearity OIP3 [dBmV]	64	63	62
Linearity OIP2 [dBmV]	80	82	83
Low-gain mode	47 MHz	450 MHz	862 MHz
Gain [dB]	8.7	8.2	7.2
Noise figure [dB] [1]	16.1	16.1	16.6
Input matching [dB]	-23	-18	-14
Linearity OIP3 [dBmV]	63	61	56
Linearity OIP2 [dBmV]	63	76	57
Triple-VCO			
VCO1 [3]	1580 - 1874 MHz		
C/N@1MHz [2]	-126 dBc/Hz		
VCO2 [3]	1869 - 2229 MHz		
C/N@1MHz [2]	-125 dBc/Hz		
VCO3 [3]	2129 - 2546 MHz		
C/N@1MHz [2]	-124 dBc/Hz		

[1]Spec. is 30dB [2]Middle of band, Tune=3V [3]Tune=0.25-4.75V

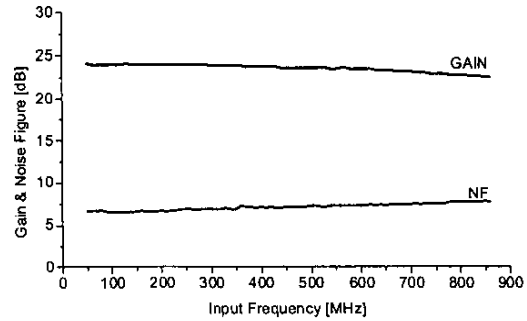

Fig. 9. Upconverter gain and noise in the high-gain mode.

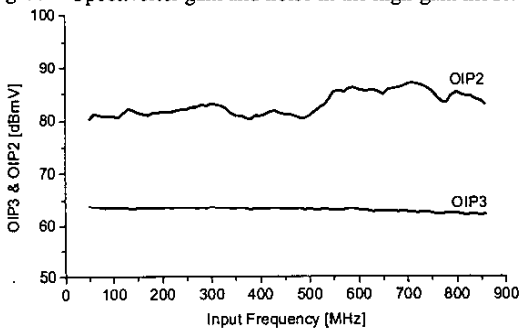

Fig. 10. Second- and third order intercept points.

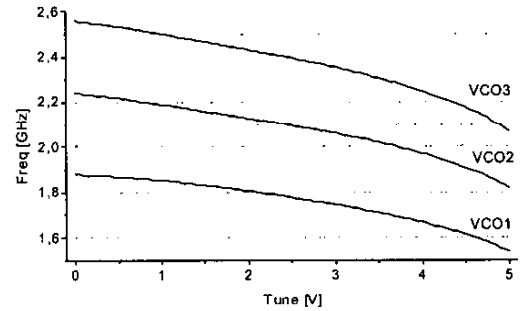

Fig. 11. Triple-VCO frequency tuning characteristics.

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